

FIG. 1A

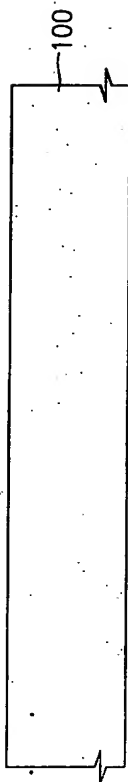


FIG. 1B

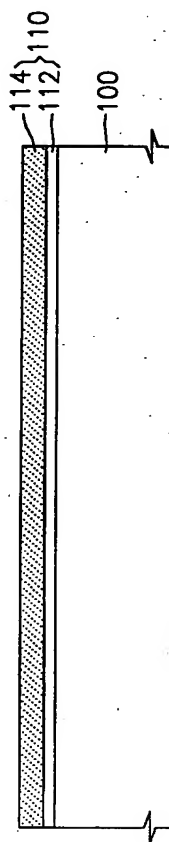


FIG. 1C

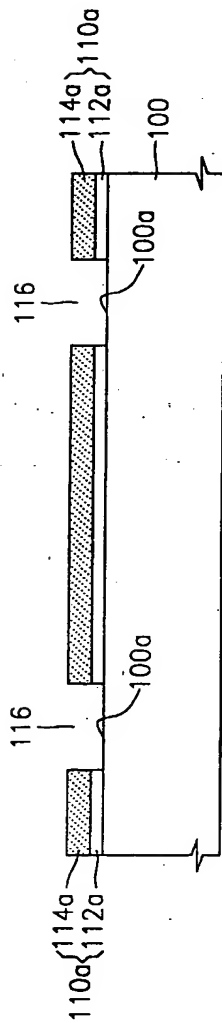


FIG. 1D

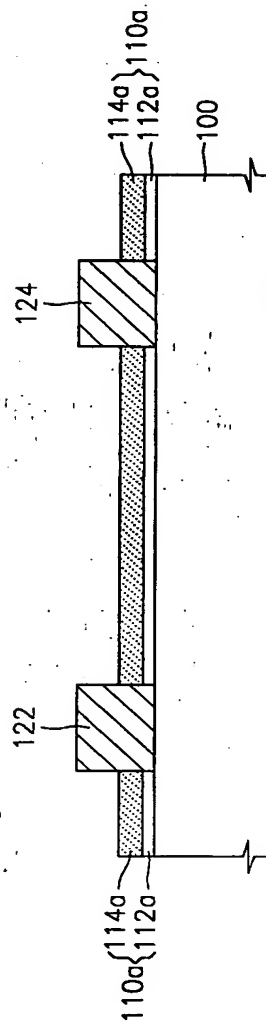


FIG. 1E

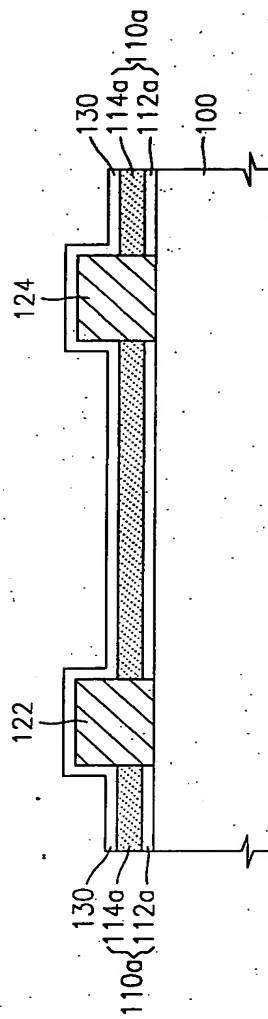
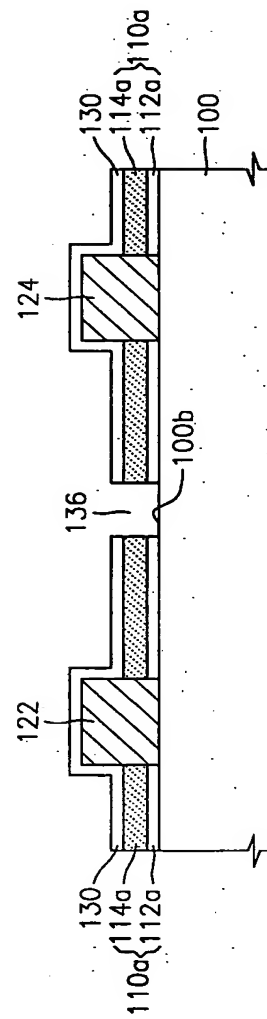


FIG. 1F



This cross-sectional view shows a semiconductor device with two gates, 122 and 124, positioned on a substrate 100. Each gate is composed of a gate dielectric layer 130, a gate electrode 110a, and a gate spacer 112a. The gates are separated by a channel region 140. The device is shown in a cross-section along the line A-A' of Figure 1.

FIG. 2A

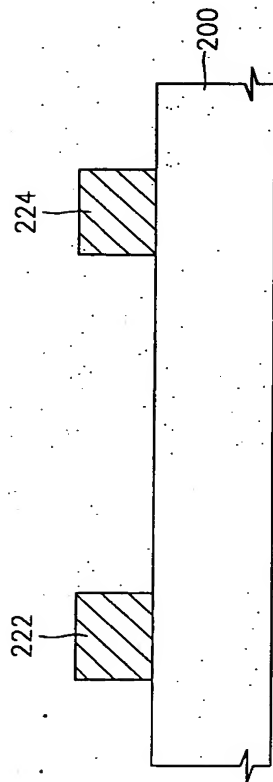


FIG. 2B

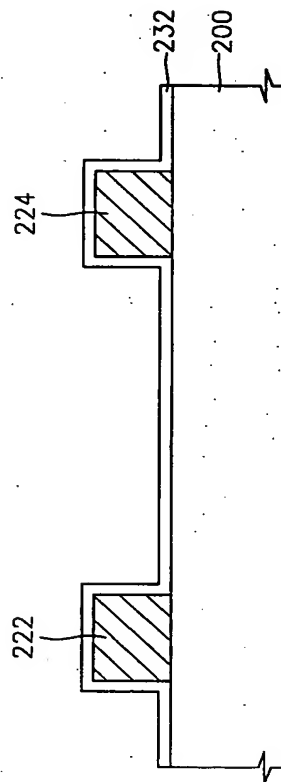


FIG. 2C

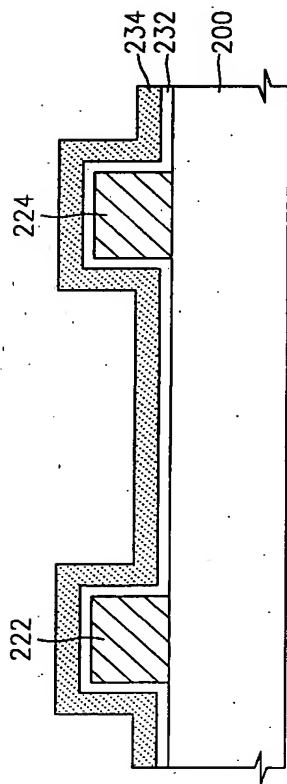


FIG. 2D

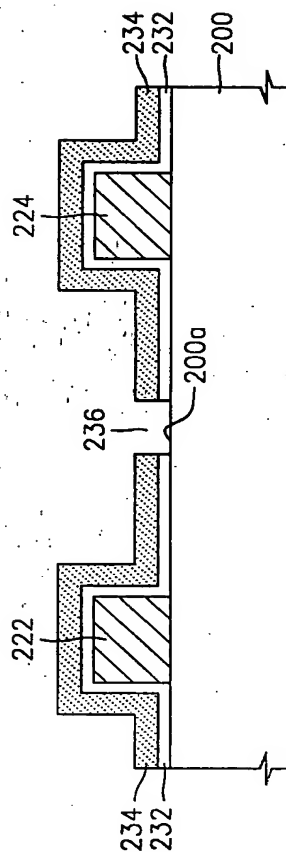


FIG. 2E

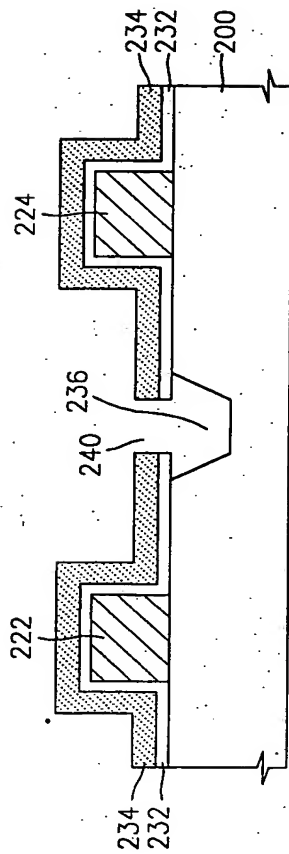


FIG. 2F

